Patent claims

1.-13. (cancelled)

14. (new) A method for programming a memory module by stimulating individual inputs of the memory module via at least one memory cell of a Boundary Scan Register (BSCAN), the method comprising:

exclusively activating such control signal input of the memory module responsible for activating or deactivating a write operation, wherein a switch-over of a WRITE ENABLE signal fed to the control signal input by the memory cell from "LOW" to "HIGH" potential or from "HIGH" to "LOW" potential is controlled using an instruction sequence fed to inputs of an update flip-flop of the memory cell, the update flip-flop generating the WRITE ENABLE signal having a "LOW" level or a "HIGH" level based on the instruction sequence.

15. (new) The method according to Claim 14, wherein the "LOW" or "HIGH" levels at the inputs of the update flip-flop can be generated in any given timing sequence.

16. (new) The method according to Claim 14, wherein the timing sequence of the "LOW" or "HIGH" levels at the setting signal input or resetting signal input of the update flip-flop is controlled by the instruction sequence.

17. (new) The method according to Claim 15, wherein the timing sequence of the "LOW" or "HIGH" levels at the setting signal input or resetting signal input of the update flip-flop is controlled by the instruction sequence.

18. (new) The method according to Claim 14, wherein the signals for the update-flip-flop are generated by a control unit based

on the instruction sequence.

19. (new) The method according to Claim 15, wherein the signals for the update-flip-flop are generated by a control unit as a function of the instruction sequence.

20. (new) The method according to Claim 16, wherein the signals for the update-flip-flop are generated by a control unit as a function of the instruction sequence.

21. (new) A method for programming a memory module by stimulating individual inputs of the memory module via at least one memory cell of a BSCAN register for generating a WRITE_ENABLE signal for the purposes of activating or deactivating a write operation, the method comprising:

automatically switching the WRITE_ENABLE signal from "LOW" to "HIGH" potential or from "HIGH" to "LOW" potential by a control unit, wherein an update flip-flop of the memory cell responsible for the generation of the WRITE_ENABLE signal is set or reset.

22. (new) The method according to Claim 21, wherein the automatic generation of a setting signal for activating the write operation can be activated by the control unit using a programming command.

23. (new) The method according to Claim 22, wherein the automatic generation of the setting signal can be prevented if specific instructions are present.

24. (new) The method according to Claim 21, wherein a further instruction is used, with which the control unit can be notified that a setting signal for activating the write operation is to be automatically generated.

25. (new) The method according to Claim 21, wherein a further instruction is used, with which the control unit can be notified that a reset signal for deactivating the write operation is to be automatically generated.

26. (new) The method according to Claim 24, wherein a further instruction is used, with which the control unit can be notified that a reset signal for deactivating the write operation is to be automatically generated.

27. (new) The method according to Claim 21, wherein the suitable point in time for automatic switchover of the WRITE_ENABLE signal is programmed by suitable instructions.

28. (new) A control unit for programming a memory module by stimulating individual inputs of the memory module via at least one memory cell of a Boundary Scan Register (BSCAN), the control unit adapted for exclusively activating a control signal input of the memory module responsible for activating or deactivating a write operation, wherein a switch-over of a WRITE ENABLE signal fed to the control signal input by the memory cell from "LOW" to "HIGH" potential or from "HIGH" to "LOW" potential is controlled using an instruction sequence fed to inputs of an update flip-flop of the memory cell, the update flip-flop generating the WRITE ENABLE signal having a "LOW" level or a "HIGH" level based on the instruction sequence.